EXPRESS MAIL LABEL NO:
EL 710 212 794 US

LEADFRAME AND SEMICONDUCTOR PACKAGE MADE USING THE LEADFRAME

Byung Hoon Ahn
Jae Hun Ku
Young Suk Chung
Suk Gu Ko
Sung Sik Jang
Young Nam Choi
Won Chul Do

BACKGROUND OF THE INVENTION

A typical package for a semiconductor chip includes an internal leadframe, which functions as a substrate for the package. The leadframe includes a central metal chip pad and a plurality of leads. A body of a hardened, insulative encapsulant material covers the chip, chip pad, and an inner portion of each of the leads. The encapsulant material is provided both above and below the chip pad and leads.

The semiconductor chip is mounted on the chip pad and is electrically connected to the leads. In particular, the chip includes a plurality of bond pads, each of which is electrically connected by a conductor (e.g., a wire) to an encapsulated inner portion of one of the leads. An outer portion of each lead extends outward from the body of encapsulant material, and serves as an input/output terminal for the package. The outer portion of the leads may be bent into various configurations, such as a J lead configuration or a gull wing configuration.

Lately, practitioners have attempted to make packages thinner by providing the chip pad and leads at a bottom surface of the body of encapsulant material, rather than in the middle of the body of encapsulant material. Such packages enjoy a lower height than the standard leadframe packages mentioned above, since there is no encapsulant beneath the chip pad and leads.

In addition, there is a demand for smaller and smaller packages. Leadframes for such packages have themselves become smaller and thinner.

SUMMARY OF THE INVENTION

The present invention includes leadframes, semiconductor packages made using the leadframes, and methods of making the leadframes and packages. The packages of the present invention can be made very thin, because the leads are exposed at a bottom surface of the encapsulant material. Moreover, the packages are reliable, because encapsulant material is provided under one or more portions of the leads, thereby locking the leads to the package body of encapsulant material. Further, encapsulant material can be provided under a peripheral lip of a chip pad upon which the chip is mounted, thereby locking the chip pad to the encapsulant material.

For instance, a metal leadframe in accordance with one embodiment of the present invention includes a rectangular frame. A chip pad is inside of and integrally connected to the frame. A plurality of leads extend from the frame toward the die pad. Each lead includes an inner end adjacent to the chip pad, an outer end integrally connected to the frame, a first surface, and a second surface opposite the first surface. The second surface of each lead is split into a first region and a second region by a groove including a recessed horizontal third surface that extends across the lead. The

first region of the second surface of the lead is between the frame and the third surface, and the second region is between the third surface and the inner end of the lead. The chip pad may include a first surface, a second surface opposite a central portion of the first surface, and a third surface opposite a peripheral portion of the first surface and surrounding the second surface. The third surface is recessed from the second surface. The first surface of the chip pad may include a groove extending in a ring adjacent to peripheral sides of the chip pad.

A semiconductor package in accordance with another embodiment of the invention may be made from such a leadframe. A semiconductor chip is mounted on the first surface of the chip pad and is in an electrical connection with the first surface of at least some of the leads. A package body of a hardened encapsulant material covers the chip, at least the first surface of the chip pad, and the first surface and third surface of the leads. The first and second regions of the second surface of the leads, and typically the second surface of the chip pad, are exposed in a plane of a first exterior surface of the package body for externally connecting the package to a motherboard or the like. Further, in the case where a groove is formed in the first surface of the die pad, the groove may surround the chip, and the chip may be electrically connected to the chip pad by a wire bonded within the groove.

These and other aspects of the present invention may be better appreciated upon consideration of the exemplary embodiments that are shown in the figures and discussed below.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1a is a top plan view of a leadframe according to a first embodiment of the present invention;

FIG. 1b is a bottom plan view of the leadframe according to the first embodiment of the present invention;

FIG. 1c is a cross-sectional side view of the leadframe according to the first embodiment of the present invention;

FIG. 2a is a bottom plan view of a leadframe according to a second embodiment of the present invention;

FIG. 2b is a cross-sectional side view of the leadframe according to the second embodiment of the present invention;

FIG. 3a is a top plan view of a leadframe according to a third embodiment of the present invention;

FIG. 3b is a bottom plan view of the leadframe according to the third embodiment of the present invention;

FIG. 3c is a cross-sectional side view of the leadframe according to the third embodiment of the present invention;

FIG. 4a is a cross-sectional side view of a semiconductor package made using the leadframe of FIGS. 1a through 1c;

FIG. 4b is a bottom plan view of the semiconductor package made using the leadframe of FIGS. 1a through 1c;

FIG. 5a is a cross-sectional side view of a semiconductor package made using the leadframe of FIGS. 2a and 2c;

FIG. 5b is a bottom plan view of the semiconductor package made using the leadframe of FIGS. 2a and 2b;

FIG. 6a is a cross-sectional side view of a semiconductor package made using the leadframe of FIGS. 3a through 3c; and

FIG. 6b is a bottom plan view of the semiconductor package made using the leadframe of FIGS. 3a through 3c.

DETAILED DESCRIPTION

The present invention will now be described in connection with the exemplary embodiments described below with reference to the accompanying drawings.

First, FIGS. 1a through 1c are a top plan view, a bottom plan view and a cross-sectional side view, respectively, of a leadframe 101 according to a first embodiment of the present invention. FIGS. 2a and 2b are a bottom plan view and a cross-sectional side view of a leadframe 102 according to a second embodiment of the present invention. FIGS. 3a through 3c are a top plan view, a bottom plan view and a cross-sectional side view of a leadframe 103 according to a third embodiment of the present invention. In FIGS. 1b, 2a, 3a, and 3b, the shaded areas are vertically recessed from the laterally

adjacent non-shaded surfaces. FIGS. 4a and 4b are a cross-sectional side view and a bottom view, respectively, of a semiconductor package 201 made using the leadframe 101 of FIGS. 1a through 1c. FIGS. 5a and 5b are a cross-sectional side view and a bottom view, respectively, of the semiconductor package 202 made using the leadframe 102 of the FIGS. 2a and 2b. Finally, FIGS. 6a and 6b are cross-sectional side view and bottom plan view, respectively, of a semiconductor package 203 made using the leadframe 103 of FIGS. 3a through 3c. In the drawings, like features typically have the same reference numbers, in which case the same discussion applies across the various embodiments.

Generally, a leadframe for a semiconductor package is manufactured by mechanically stamping or chemically etching continuous metal strips.

The leadframes 101, 102 and 103 may be made of a common leadframe metal, such as copper(Cu), copper alloy(Cu Alloy), Alloy 37 (nickel(Ni) 37% and steel(Fe) 55%) and copper-plated steel, according to the application.

Referring to leadframe 101 of FIGS. 1a, 1b, and 1c, a plate type frame 2, which encloses a space of a prescribed size, is formed at the center of the leadframe. A rectangular chip pad 6 is at the center of the space within the frame is connected at its four corners and supported by four tie bars 4. Each tie bar 4 is integrally connected between an inner end of any one of a plurality of leads 8 extending inward from the frame 2 and a corner of chip pad 6. In this example, the tie bars 4 are each integrally connected to a lead 8 that is adjacent to a corner of frame 2.

A plurality of leads 8 extend inward from frame 2. An outer end of each lead 8 is integrally connected to the frame 2 and the opposite inner end of the lead 8 is either

connected to a tie bar 4 or is a free end that extends to a point adjacent to, but not contacting, chip pad 6.

In leadframe 101, the inner end of the leads 8 that are not connected to a tie bar 4, i.e., the free inner ends, extend from frame 2 toward chip pad 6. There are 32 such leads 8, with eight leads 8 between pairs of the tie bars 4.

The free end of some of the leads 8 that are directed toward chip pad 6 are bent at angles toward chip pad 6. The bend helps to lock the lead 8 to encapsulant material later applied to the leadframe. Each lead 8 may have an anchor ear 10 projecting from a side of the lead 8. The anchor ear 10 serves to restrict an encapsulant 18 (see FIG. 4a) in the finished semiconductor package as well as to prevent the lead 8 from being pulled out from encapsulant 18 horizontally or vertically. Selectively, to further restrict the encapsulant 18, a concave hole or a depressed part may be formed in the lead 8 in place of the anchor ear 10. It will be appreciated that the anchor ear 10 is optional.

Here, the number, position and path of the leads 8 of the leadframes 101, 102 and 103 described herein are exemplary only, and may be changed according to the application. Furthermore, the leads 8 may be designed suitable for the number and position of input-output pads 14 of a semiconductor chip 12 (see FIG 4a) to be mounted on the leadframe. Additionally, in the drawings, the leadframes 101, 102 and 103 are in the form of a square, but may be in the form of a non-equilateral rectangle. Moreover, in the drawings, the leads 8 are formed adjacent to all four sides of chip pad 6, as in a quad package, but may be formed adjacent to only two parallel sides of chip pad 6, as in a dual package. Also, only two tie bars 4 may be formed to support chip pad 6. Further, the tie

bars 4 may be integrally connected between frame 2 and chip pad 6 rather than between a lead 8 and chip pad 6.

Chip pad 6 of leadframe 101, 102, and 102, includes a first surface 6a of approximately flat type, a second surface 6b of approximately flat type opposed to a central portion of first surface 6a, and a third surface 6c of approximately flat type opposed to a peripheral portion of the first surface 6a. The third surface 6c is vertically recessed in a predetermined interval from the second surface 6b. Third surface 6c extends fully around second surface 6b and chip pad 6, so as to form a lip beginning at first surface 6a and ending a selected distance from second surface 6b.

A center area of the chip pad 6 has a first thickness between the first surface 6a and the second surface 6b. A peripheral area around chip pad 6 has a second thickness between first surface 6a and third surface 6c that is less (e.g., about half) than the first thickness. The shaded parts in FIGS. 1b, 2a, and 3a indicate the third surface 6a in an embodiment where third surface 6c circumscribes chip pad 6.

Alternatively, with reference to FIGS 3a and 3c, chip pad 6 may have a groove bottomed by a horizontal fourth surface 6d formed in the first surface 6a and leadframe 103 opposed to the second surface 6b. Fourth surface 6d is depressed a predetermined depth in a peripheral region of first surface 6a, and the semiconductor chip 12 is mounted inward of the groove (see FIG. 6a). For an example, the groove having fourth surface 6d may be in the form of a rectangular ring located inward of third surface 6c adjacent a periphery of chip pad 6, with chip 12 located within the ring (see FIGS. 3a, 3c, and 6b).

The shaded part of FIGS. 1b, 2a, 3b and tie bar 4 have the same second thickness as is between the first surface 6a and the third surface 6c of the chip pad 6. That is, the underside of tie bars 4 also are recessed.

Referring to FIGS. 1c, 2b, and 3c, the lead 8 includes a first surface 8a of approximately flat type and a second surface 8b of approximately flat type opposed to the first surface 8a. In FIGS. 1c, 2b, and 3c, the reference letter S indicates a virtual sawing line through leads 8 where the leads are cut during a manufacturing process to singulate the semiconductor package. The package also can be singulated by punching through the leads 8 at line S.

Referring to leadframe 101 of FIGS. 1b and 1c, a horizontal recessed third surface 8c may be provided opposite first surface 8a in a groove in second surface 8b across lead 8. Therefore, two regions of second surface 8b exist on each lead on either side of third surface 8c. The first region of second surface 8b is between frame 2 and third surface 8c and the second region of second surface 8c is between third surface 8c and the inner end of lead 8. Optionally, a horizontal fourth surface 8d may be provided opposite first surface 8a and recessed from second surface 8b beginning at the inner end of the lead 8 immediately adjacent to chip pad 6. Anchor ears 10 also are recessed from second surface 8b of lead 8.

Referring to leadframe 102 of FIGS. 2a and 2b, the recessed horizontal third surface 8c of the leads 8 also may be formed in an area of the second surface 8b close to frame 2 and at sawing line S, so that there is only one region of second surface 8b. Optionally, a recessed horizontal fourth surface 8d may be formed beginning at the inner end of the lead 8 adjacent chip pad 6 and extending to second surface 8b, as described

above. In this embodiment, the single area of second surface 8b is fully inward of the inner and outer ends of the lead 8.

Referring to leadframe 103 of FIGS. 3b and 3c, second surface 8b extends to sawing line S and frame 2. A horizontal fourth surface 8d is recessed from second surface 8b at the inner end of the lead 8. Anchor ear 10 also is recessed from second surface 8b. There is no third surface 8c as in leadframe 101.

Referring to FIGS. 1c, 2b, and 3c, leads 8 have a first thickness between first surface 8a and second surface 8b, and a lesser second thickness (e.g., 50% less) between first surface 8a and the recessed third and fourth surfaces 8c and 8d. Typically these first and second thicknesses of leads 8 are the same as the first and second thicknesses mentioned above for chip pad 6.

In packages made from leadframe 101, 102, and 103, the second surface 8b formed either as one or two regions on the leads 8 serves to electrically connect the semiconductor package 201, 202, and 203 (see FIGS. 4a, 4b, 6a, 5b, 6a, and 6b) to the mother board, thereby indirectly connecting packaged chip 12 to the motherboard. The first surface 6a, the recessed third surface 6c and the optional fourth surface 6d of the chip pad 6, and the first surface 8a, the recessed third surface 8c, and the recessed optional fourth surface 8d of the lead 8 are all located inside encapsulant 18. The recessed lower third surfaces 6c, 8c, and fourth surface 8d are underfilled by encapsulant 18. The thickness of the chip pad 6 and the leads 8 of the leadframes 101, 102 and 103 may be about 0.15mm to 0.50mm and the depth of the recess formed by the third surfaces 6c, 8c, fourth surface 8d, and fourth surface 6d may be about 0.075mm to 0.25mm. As the percentage, the depth of the recessed part formed by the third surfaces 6c, 8c, fourth

surface 8d, and the fourth surface 6d may be about 50% or 33% to 75% of the total thickness of the chip pad 6 or lead 8. Of course, these values are example values. Real values may be changed according to the application.

The leadframes 101, 102 and 103 may be formed of a milled metal strip by a common chemical wet etching process. As known, chemical etching (called also chemical milling) uses photolithography, photoresist and a chemical solution for etching a pattern into the metal strip are used. Generally, the photoresist layer is formed on one side or two sides of the strip. Next, the photoresist layer is exposed to light through a mask, on which a desired pattern is formed. The chemical solution is applied to the one or two sides of the strip. The exposed areas of the strip are etched and removed, and thereby the desired pattern remains in the metal strip.

By performing the etching twice, the leadframes 101, 102 and 103 can be formed. The first etching step is carried out on the one or two sides of the strip through a photoresist pattern on the one or two sides of the strip. The first etching step completely passes through predetermined regions of the metal strip in order to form the overall pattern of leadframes 101, 102 and 103.

Next, to form the recessed regions, a second photoresist pattern is formed on predetermined areas of one side or two sides of the leadframes 101, 102 and 103. For example, a circumferential area of the chip pad 6 and a selected area of the lead 8 are not covered by the second photoresist pattern, and therefore, are etched by a second etching step. The second etching step is carried out on the one or two sides of the leadframes 101, 102 and 103 through the second photoresist pattern. As shown in FIGS. 1b, 1c, 2a, 2b, 3a and 3b, in the second etching step, the depressed surfaces are formed in the

leadframes 101, 102 and 103. For example, the third surface 6c and the fourth surface 6d of chip pad 6, and third surfaces 8c and fourth surface 8d of the leads 8 are formed during the second etching step. Anchor ears 10 and tie bars 4 are also partially removed in their thicknesses by the second etching step.

During the second etching step, after the chemical solution removes a desired amount of the vertical thickness of the chip pad 6, leads 8 anchor ears 10, and tie bars 4, the second etching step is stopped. The second etching step is carried out in such a manner that the recessed lower surfaces of chip pad 6 and leads 8 will be within encapsulant 18 of the package to be formed with leadframes 101, 102, and 103 (see FIGS. 4a, 5a, and 6a), e.g., the encapsulant 18 fills in under the third surface 6c of the chip pad 6 and the third surface 8c and fourth surface 8d of the leads 8.

In general, in the second etching step, the thickness of the selected areas of chip pad 6 and leads 8 is removed to about 50% of their original thickness, but the amount removed may be within the range of about 33% to 75% of the thickness of the leadframe, depending on the application.

The second surface 6b of chip pad 6 and the inner end of second surface 8b of leads 8 have rounded inner ends in the embodiments shown in FIGS. 4b, 5b, and 6c. This may reduce package stresses.

Additionally, the leadframes 101, 102, or 103 may be formed by a first step of mechanically stamping the whole pattern of the leadframe and by a second step of chemically etching partially through the chip pad 6 and the lead 8 of the stamped leadframe and other portions of the leadframe to form the recessed surfaces.

Meanwhile, after the etching step, the first surface 8a of the lead 8 of the leadframes 101, 102 and 103 may be plated with metal, such as gold(Au), silver(Ag), nickel(Ni), palladium(Pd), copper(Cu) and others, in order to better bond to conductive wires 16 of the package (see FIGS. 4a, 5a, and 6a). Furthermore, to facilitate connection of the second surface 8b of the leads 8 to the mother board, the second surface 8b may be plated with a metal such as gold, nickel, palladium, inconel, solder of lead and tin, or tantalum.

Referring to FIGS. 4a and 4b, the semiconductor package 201 includes chip pad 6 and a plurality of leads 8. The chip pad 6 has the first surface 6a of approximately flat type, the second surface 6b of approximately flat type opposite a central portion of first surface 6a, and the encapsulant-covered third surface 6c of approximately flat type. The third surface 6c is opposed to a peripheral portion of the first surface 6a fully around second surface 6b. The third surface 6c is vertically recessed from second surface 6b.

The leads 8 of semiconductor package 201 extend toward the chip pad 6 without contacting to the chip pad 6. Each lead 8 has the first surface 8a of approximately flat type, the second surface 8b of approximately flat type, the third surface 8c of approximately flat type, and an optional fourth surface 8d of approximately flat type. The second surface 8b, the third surface 8c and the fourth surface 8d are opposed to respective portions of the first surface 8a. The third surface 8c and fourth surface 8d are vertically between the first surface 8a and the second surface 8b, i.e., are vertically recessed from second surface 8b.

Here, the frame of the leadframe is removed along the sawing line S (see FIG. 1c) in a sawing step or punching step of the manufacturing process of the semiconductor

package, wherein a finished package is singulated from the strip of leadframes. A small stub including the outer end of leads 8 may extends beyond the peripheral sides of encapsulant 18.

Referring to FIGS. 4a and 4b, third surface 8c is within a horizontal groove that splits second surface 8c between the peripheral edge of encapsulant 18 and fourth surface 8d. Fourth surface 8d begins at the inner end of the lead 8 adjacent chip pad 6 and extends a short distance outward toward the periphery of encapsulant 18. Fourth surface 8d is covered by encapsulant 18. Since third surface 8c is at an intermediate portion of lead 8, the second surface 8b, which is exposed at the lower exterior surface of package 201, is split into two exposed regions by the encapsulant 18 that covers third surface 8c. Fourth surface 8d is formed by etching partially through lead 8 in a manner that leaves the inner end of the exposed inner region of second surface 8b with a rounded profile.

A semiconductor chip 12, into which various electronic circuits are integrated, is mounted on the center of the first surface 6a of the chip pad 6 and is attached with a bonding means 22. The semiconductor chip 12 has a plurality of input-output pads 14 formed on an active upper surface thereof. The bonding of the semiconductor chip 12 to chip pad 6 may be performed with common semiconductor chip bonding means, such as common epoxy adhesives, adhesive films or adhesive tapes.

Some or all of the input-output pads 14 of the semiconductor chip 12 are electrically connected to the first surface 8a of a respective one of the leads 8 by a conductive wire 16 or equivalent conductor. Here, as described above, the first surface 8a of the lead 8 may be plated with a common metal, such as gold, silver, nickel, palladium, copper or others to such facilitate bonding.

A hardened body of an adhesive encapsulant material seals the chip pad 6, the semiconductor chip 12, the conductive wire 16 and the leads 8. That is, the hardened encapsulant covers the semiconductor chip 12, the conductive wires 16, the sides of the chip pad 6, the first and third surfaces 6a and 6c of the chip pad 6, and the first, third surfaces and fourth surfaces 8a, 8c and 8d and the peripheral sides of the leads 8. The second surface 6b of the chip pad 6 and the two regions of second surface 8b of the leads 8 are not covered with the encapsulant 18 but rather are exposed to the outside in the horizontal plane of the lower exterior surface of the body of encapsulant 18. Depending on the location of sawing line S, the outer region of second surface 8b of leads 8 can extend beyond the perimeter of encapsulant 18 onto an outer stub of the severed lead 8.

Here, by having third surface 8c and fourth surface 8d covered by encapsulant 18, leads 8 are locked to encapsulant 18. Further, by having third surface 6c around exposed second surface 6b of chip pad 6 covered by encapsulant 18, chip pad 6 is locked to encapsulant 18. That is, the leads 8 and chip pad 6 are prevented from being separated from the encapsulant 18 horizontally or vertically.

Moreover, by having a narrow fourth surface 8d at the inner end of leads 8, and by forming a narrow third surface 8c at an intermediate area of a longitudinal direction of the lead 8, vibration or bending of the lead 8 during the wire bonding or molding process is prevented while maintaining a secure lock between encapsulant 18 and leads 8. That is, generally, a vibration or bending of the lead 8 can occur during the wire bonding or molding process. Such vibration or bending can be avoided by forming fourth surface 8d longitudinally short or, optionally, omitted it altogether. For example in FIGS. 4a, 5a,

and 6a, fourth surface 8d is fully inward of the point of connection of wire 16 to first surface 8a of lead 8.

There are various methods for forming the body of encapsulant 18. For example, the body of encapsulant 18 may be formed using a common plastic molding technique. In such method, the leadframe is located in a transfer or injection mold and encapsulant material is provided on the upper surface of the leadframe and subsequently cured. The molding process is done in a manner that underfills third surface 6c of chip pad 6 and third and fourth surfaces 8c and 8d of leads 8, while leaving second surface 6b of chip pad 6 and second surface 8b of leads 8 uncovered and exposed. The encapsulant may be a common epoxy molding compound. As examples of molding compounds include NITTO MP-8000AN™ molding compound provided by the Nitto Company in Japan and EME 7351 UT™ provided by the Sumitomo Company in Japan. A side of the mold is tapered, resulting in a taper on the peripheral sides of the body of encapsulant 18, so that the encapsulated leadframe can be easily removed from the mold. Typically, the body of encapsulant 18 is individualized, that is, molded as a distinct unit over each leadframe 18. Accordingly, the leadframe may be sawed or punched around the respective body of encapsulant 18 along sawing line S through leads 8 inside of frame 2.

Instead of the molding method, a liquid-type encapsulating method may be used. For example, in a first step, the leadframe is located on a horizontal surface. In a second step, a common contact bead of hardenable adhesive material, such as HYSOL 4451™ epoxy provided by the Dexter-Hysol Company of City of Industry in California, can be coated on the leadframe to form a closed angle dam at a predetermined area of the lead around the semiconductor chip. In a third step, the bead is hardened by a process, such as

heating at a temperature of about 140 degrees for an hour. In a fourth step, the hardenable liquid-type encapsulating material, such as HYSOL™ 4450 liquid type encapsulant material, is poured over the leadframe the inside of the bead to form the package body. In a final step, the poured liquid-type encapsulant is hardened, for example, by heating at a temperature of about 140 degrees for an hour. Typically, all leadframes of the strip would be encapsulated in one block of encapsulant, although each leadframe also could be encapsulated in an individual block of encapsulant 18. Subsequently, a sawing step is carried out along line S for singulating the individual packages from the block of encapsulant over the strip of leadframes.

Specific areas of the leadframe that are not covered with the encapsulant 18, such as the second surface 6b of the chip pad 6 and the second surface 8b of the lead 8, may be plated with a common plating metal or metals, such as gold, nickel, palladium, inconel, solder of lead and tin, or tantalum. Such plating may be performed in the step of manufacturing the leadframe. The plated regions may easily be soldered to a motherboard.

Practitioners will appreciate that chip pad 6 can be up set during the encapsulation process, so that second surface 6c is covered by encapsulant 18 in the semiconductor package.

Referring to FIGS. 5a and 5b, the semiconductor package 202 is very similar to package 201 of FIGS. 4a and 4b, having common parts and reference numbers, and hence needs only be described with respect to differences from the semiconductor package 201.

In semiconductor package 202 of FIGS. 5a and 5b, the leads 8 of leadframe 102 of FIGS. 3a, 3b, and 3c have a recessed third surface 8c extending between second

surface 8b and sawing line S adjacent frame 2. As shown in FIG. 5b, the one region of exposed second surface 8b of the lead 8 is located fully within the peripheral sides of the body of encapsulant 18, since third surface 8c is covered by encapsulant 18 and is between second surface 8b and the adjacent package side. An optional fourth surface 8d is formed at the inner end of lead 8 opposite the third surface 8c at the outer end of the lead 8, such that third surface 8c and fourth surface 8d are covered by encapsulant 18. Accordingly, the locking force or binding force between the lead 8 and the encapsulant 18 is enhanced.

Generally, a bur may be generated by a punching step performed after encapsulation to singulate an individually encapsulated packages from the leadframe strip. The bur (not shown) is directed downward at the line of cut through lead 8. In the case of leadframe 102 and package 202, however, the effect of any bur is minimized by providing third surface 8c at cutting line S and away from second surface 8b. Any such bur would therefore be formed at third surface 8c and not as second surface 8b. Since second surface 8b is free of any such bur, semiconductor package 202 may be mounted easier to a motherboard.

Referring to FIGS. 3a, 3b, 6a and 6b, the semiconductor package 203 made from leadframe 103 is similar to semiconductor package 201 and has similarly numbered features. Thus, semiconductor package 203 need only be discussed in terms of its differences.

As shown in the drawings, the leadframe 103 and package 203 further includes the flat-type fourth surface 6d at the bottom of a rectangular groove formed in the first surface 6a of the chip pad 6 on which the semiconductor chip 12 is mounted. Fourth

surface 6d is vertically recessed from first surface 6a, and in this embodiment surrounds chip 12.

In one application, one or more input-output pads 14 for ground or some other voltage of the semiconductor chip 12 are electrically connected to the fourth surface 6d by a conductive wire 16, as is shown in FIG. 6a. In such an application, bonding means 22 may be electrically insulative to isolate the backside of chip 12, or bonding means 22 may be electrically conductive to apply a backside potential to chip 12. Further, the exposed second surface 6b of chip pad 6 may be electrically connected by solder, solder paste, or an electrically conductive adhesive to a ground or other voltage terminal of a motherboard.

By having the fourth surface 6d located in a groove of first surface 6a of chip pad 6, the chip pad 6 is bonded and bound to the encapsulant 18 more strongly because of the increased surface area provided by the groove. Furthermore, by bonding the conductive wires 16 to fourth surface 6c within the groove, the conductive wires 16 are prevented from being separated from the fourth surface 6d of the chip pad 6, which might otherwise occur due to thermal expansion or molding.

Of course, the fourth surface 6d of the chip pad 6 may be plated with a metal, such as gold, silver, nickel, palladium and copper, so as to strengthen the bond to conductive wires 16.

In package 302 of FIGS. 6a and 6b, fourth surface 8d of the lead 8 is formed only at the inner end of the leads 8 adjacent to chip pad 6. There is no third surface 8c as in semiconductor packages 201 and 202. The exposed second surface 8b of lead 8 extends

longitudinally from fourth surface 8c to the outer end of lead 8 that is at or just beyond the peripheral edge of encapsulant 18.

Practitioners will appreciate that a chip pad 6 having a groove bottomed by a fourth surface 6d, and one or more conductive wire(s) connected therein, as in FIGS. 6a and 6b, could be substituted into the semiconductor packages 201 and 202.

Therefore, according to embodiments of the present invention, the leadframes semiconductor packages made therewith have leads with one or more undercuts in its lower surface, thereby forming recessed horizontal surfaces, which subsequently are underfilled with encapsulant material, thereby improving the bonding force and binding force between the lead and the package body.

Furthermore, the chip pad may have a recessed fourth surface formed in the upper surface of the chip pad upon which the semiconductor chip is mounted. The fourth surface is in a groove that is encapsulated, thereby improving the bonding force and binding force between the chip pad and the encapsulant.

Moreover, to improve the binding force between the leads and the encapsulant, a recessed third surface can be formed across the lead at a center area of the longitudinal direction of the lead, or at an area of lead adjacent at the side of the package, thereby preventing the vibration or bending of the lead during the wire bonding or molding process and better locking the lad to the package body.

Additionally, if the recessed third surface of the leads is formed where the leads are cut by punching during package singulation, then a bur that may be formed during the punching step will not be located on the second surface of the lead that is electrically

connected to the mother board. Accordingly, the semiconductor package can be contacted to the mother board more closely, thereby increasing the mounting efficiency.

Furthermore, when the recessed fourth surface is formed in a groove in an upper top surface of the chip pad, and one or more wires are bonded to the fourth surface within the groove, then the strong bond between the fourth surface and the encapsulant in the recess helps control the heat expansion and prevent the separation of the conductive wire from the fourth surface.

While the present invention has been described with reference to the particular illustrative embodiments, it is not to be restricted to the embodiments but only by the appended claims. It is to be appreciated that those skilled in the art can change or modify the embodiments without departing from the scope and spirit of the present invention.